CLAIM AMENDMENTS

1. ~~(Original) A method~~ comprising:

defining a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

managing the core from said region.

2. (Original) The method of claim 1 including managing the core from a level 2 cache.

3. (Original) The method of claim 1 including using a virtual address to index the core to avoid the need for an address translation mechanism.

4. (Original) The method of claim 1 including placing functions relating to tags and valid bits as well as the data itself in the core.

5. (Original) The method of claim 1 including using a write-through core cache.

6. (Original) The method of claim 1 including implementing a line replacement policy in said region.

7. (Original) The method of claim 1 including performing virtual-to-physical ~~translation~~ in said region.

8. (Currently Amended) The method of claim 1 including handling a core cache miss by passing [[the]] details of an [[the]] access to said region.

9. (Original) The method of claim 8 including enabling said region to use a memory translation mechanism to determine the physical address and attributes of the access.

10. (Currently Amended) The method of claim 9 including checking to see if [[the]] requested data is in a storage associated with said region.

11. (Original) An article comprising a medium storing instructions that enable a processor-based system to:

define a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

manage the core from said region.

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12. (Original) The article of claim 11 further storing instructions that enable the processor-based system to manage the core from a level 2 cache.

13. (Original) The article of claim 11 further storing instructions that enable the processor-based system to use a virtual address to index the core to avoid the need for an address translation mechanism.

14. (Original) The article of claim 11 further storing instructions that enable the processor-based system to access functions relating to tags and valid bits as well as the data itself in the core.

15. (Original) The article of claim 11 further storing instructions that enable the processor-based system to use a write-through core cache.

16. (Original) The article of claim 11 further storing instructions that enable the processor-based system to implement a line replacement policy in said region.

17. ~~(Original) The article of claim 11 further storing instructions that enable the processor-based system to perform virtual-to-physical translation in said region.~~

18. (Currently Amended) The article of claim 11 further storing instructions that enable the processor-based system to handle a core cache miss by passing [[the]] details of an [[the]] access to said region.

19. (Original) The article of claim 18 further storing instructions that enable the processor-based system to enable said region to use a memory translation mechanism to determine the physical address and attributes of the access.

20. (Currently Amended) The article of claim 19 further storing instructions that enable the processor-based system to check to see if [[the]] requested data is in a storage associated with said region.

21. (Original) A system comprising:

a processor;

a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

a storage coupled to said processor storing instructions that enable the processor to manage the core from said region.

22. (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to manage the core from a level 2 cache.

23. (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to use a virtual address to index the core to avoid the need for an address translation mechanism.

24. (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to place functions relating to tags and valid bits as well as the data itself in the core.

25. (Original) The system of claim 21 wherein said core cache is a write-through cache.

26. (Original) The system of claim 21 wherein said storage stores instructions that enable the processor to implement a line replacement policy in said region.

27. ~~(Original) The system of claim 21~~ wherein said storage stores instructions that ~~enable the processor to perform virtual-to-physical translation~~ in said region.

28. (Currently Amended) The system of claim 21 wherein said storage stores instructions that enable the processor to handle a core cache miss by passing [[the]] details of an [[the]] access to said region.

29. (Original) The system of claim 28 wherein said storage stores instructions that enable the processor to enable said region to use a memory translation mechanism to determine the physical address and attributes of the access.

30. (Currently Amended) The system of claim 29 wherein said storage stores instructions that enable the processor to check to see if [[the]] requested data is in a storage associated with said region.